APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,336	08/18/2003	Mark Justin Moore	56162.000414	1936

21967   7590   05/16/2007

HUNTON & WILLIAMS LLP
INTELLECTUAL PROPERTY DEPARTMENT
1900 K STREET, N.W.
SUITE 1200
WASHINGTON, DC 20006-1109

EXAMINER
KAWSAR, ABDULLAH AL

ART UNIT	PAPER NUMBER
2109	

MAIL DATE	DELIVERY MODE
05/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>08/18/2003</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>18 August 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>11/18/2003</u>.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____ .

DETAILED ACTION

Priority

1.   The provisional priority date of 08/16/2002 for the application has been considered.

2.   Claims 1 – 16 are pending

Specification

3.   Specification is objected as on page 6 lines 11 and 12 reads "timing precision is reduced

from a 10 micro-second level to a 100 microsecond level.", appropriate correction is required.

Claim Objections

4.   Claim 7 is objected to because of the following informalities: "slot in the rung to be

processed". Appropriate correction is required.

Claim Rejections - 35 USC § 112

5.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the
> subject matter which the applicant regards as his invention.

6.   Claims 1 – 16 are rejected under 35 USC 112, 2nd. The body of claim 1 does not perform

what set forth in the preamble. Claim calls for scheduling threads and timer mechanism of the

events, however the body of claim 1 does not schedule any threads and timer mechanism. Also

the limitations of the claim do not link to each other. There is no relationship between element

1,2 and 3 in the claims.

Claim Rejections - 35 USC § 101

7.   35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8.   Claims 1 – 16 are directed non-statutory subject matter. While scheduling threads and

timer mechanism could be reasonably tangible result, it appears the claims 1 and 9 do not

produce a claimed result to form the basis statutory subject matter under 35 USC 101.

Claim Rejections - 35 USC § 103

9.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10.   Claims 1, 2, 8, 9, 10 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Larson(US Patent No. 6,754,690)in view of "A firm real-time system implementation using

commercial off-the-shelf hardware and free software" (Srinivasan) .

As per claim 1, Larson discloses:

- a method of scheduling threads and timer mechanisms of events in a computer system (col 1 lines 43-46, "The application scheduling method of the present invention allows integration of critical real-time functions such as avionics display and control, while ensuring that the applications providing these functions are executed in a timely manner.") application scheduling method is the thread scheduling method in a timely manner(timer mechanism).

- allowing aggregation of said events to improve performance (col 3 lines 8 - 14 "eliminates the need for tracking the interrupt inter-arrival rate by (1) activating a thread in response to an interrupt; (2) associating a time period with the interrupt; and (3) ensuring that during that period the aggregate CPU utilization") allowing aggregation to for CPU utilization which improves performance.

- avoiding excessive processor overhead resulting from entry and exit interrupts (col 3 lines 18 – 20 "the arrival of an interrupt and the termination of the interrupt handling are treated as a pseudo-thread activation.") entry and exit of interrupts (col 1 lines 54-60 "The amount of CPU time available to a thread during a given period of its execution is guaranteed by the present method, which efficiently apportions available CPU time by interrupt masking and thread budgeting.") interrupt masking helps efficiency of CPU time which means avoiding excessive CPU overhead.

However Larson does not disclose a *timer mechanism allows micro-second level*

accuracy.

On the other hand Srinivasan discloses:

- implementing a timer mechanism that allows a micro-second level accuracy (sec 3.1

col 6 lines 32-33 "is a mechanism by which timer interrupts are allowed to occur at any

microsecond")

Therefore, it would have been obvious to a person of ordinary skill in art at the time of

invention was made to incorporate the teaching of Srinivasan into the method of Larson to have a

timer mechanism with micro-second level accuracy. The modification would have been obvious

because one of the ordinary skills of the art would want to perform interrupt execution more

precisely without taking CPU overhead for long interval between consecutive interrupts

execution.

As per claim 2, the rejection of claim 1 incorporates and further Srinivasan discloses:

- wherein the timer mechanism is a ring structure with an associated control block (

sec 3.2 col 8 lines 46 – 48, "Once the scheduling is begun, KURT will allow the application to

run and cause the periodic loop to execute.) kurt is the associated control block that associates

with the periodic loop execution(ring structure).

As per claim 8, the rejection of claim 1 incorporates and further Larson discloses:

- wherein the control block contains addresses corresponding to a first ring entry, a

total number of entries, and an entry for a time period between adjacent ring entries for

queuing basic operations. (Col 5 lines 18-26 "This is accomplished by associating a period

counter (PeriodCtr) with each period p, and a "last executed counter value" (ThreadCtr), with

each thread n. As shown in FIG. 2, at step 210, the thread counter for thread B, ThreadCtr (1), is

incremented to a value of 1. ThreadCtr (n) is thus set to the same value as PeriodCtr (p(n))

[where (p(n)) is period 1, thread n's period], to indicate that the budget for thread (n) has been

replenished for its period.") period counter is the control block with each period(total number of

entries) and last executed counter value is the value of first ring entry with budget(time between

adjacent entries) for each thread.

Claims 9,10 and 16 are computer readable medium comprising instructions for executing

the method of claims 1,2 and 8 above. They are therefore rejected under the same rational.

11.   Claim 3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Larson(US Patent No. 6,754,690)in view of "A firm real-time system implementation using

commercial off-the-shelf hardware and free software" (Srinivasan) further in view of Haubursin

et al.(US Patent No. 6,115,779) .

As per claim 3, Larson in view of Srinivasan discloses all the elements of claim 3 except

triggering a monostable timer to gate interrupt enables to batch servicing of interrupt request.

As per claim 3, the rejection of claim 1 incorporates and further Haubursin discloses:

- wherein implementing the timer mechanism includes triggering a monostable timer to gate interrupt enables to batch servicing of interrupt requests. (Col 7 lines 52 – 54, "The batch timer start signal produced at the output of the AND gate 116 activates the batch timer 134 decremented at a rate set by the local clock signal.") batch timer is the monostable timer with gate that starts(triggered) (col 7 lines 59 - 63 "the batch timer 134 causes the interrupt request signal to be produced when a predetermined time interval has elapsed since the occurrence of an interrupt event processed in the batch mode.") batching interrupt services.

Therefore, it would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Haubursin into the method of Larson and Srinivasan to have a timer mechanism with monostable timer to gate interrupt services. The modification would have been obvious because one of the ordinary skills of the art would want to perform interrupt execution in batching services for better execution time and scheduling.

Claim 11 is computer readable medium comprising instructions for executing the method of claim 3 above. Therefore claim 11 is rejected under the same rational.

12.   Claim 4 – 7 and 12 - 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larson(US Patent No. 6,754,690)in view of "A firm real-time system implementation using commercial off-the-shelf hardware and free software" (Srinivasan) and further in view of Lam (US Patent No. 6,782,461) .

As per claim 4, Larson in view of Srinivasan discloses all the elements of claim 4 except *generating an array of ring slots that permits the implementation of a circular array queue.* On the other hand Lam discloses:

- wherein the timer mechanism includes generating an array of ring slots that permits the implementation of a circular array queue. (col 2 lines 27 - 28, "A circular queue usually consists of an array that contains the items in the queue.") the circular queue array is the array of ring slots that contains items(events).

Therefore, it would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Lam into the method of Larson and Srinivasan to have a timer mechanism with circular queue. The modification would have been obvious because one of the ordinary skills of the art would implement a circular queue to store timer event data as it is cyclical data and improves access efficiency of timer events.

As per claim 5, the rejection of claim 4 incorporates and Lam further discloses:

. *- wherein the circular array queue is structured as a last in, first out (LIFO) queue.* (col 2 lines 39 – 42 "Circular queue 1 and circular queue 2 are each comprised of an input pointer and an output pointer that are incremented each time that a data element is processed" and in lines 44- 46 "A last-in/first-out ("LIFO") method is another possible method for data element processing")

As per claim 6, the rejection of claim 4 incorporates and Larson further discloses:

> *- including setting a number of timer events in the ring slots that invokes handler functions that include a terminating event function.* (col 5 lines 34-40 "the thread invokes the thread relinquishment service, at step 240; (2) the thread budget is exhausted, at which point an interrupt is generated by a thread timer interrupt; or (3) a period timer interrupt (signaling that a period boundary has been reached) or other interrupt occurs.")thread relinquishment service is the handler function that invokes the thread timer interrupt(terminal event function) when thread budget(timer event) is exhausted.

As per claim 7, the rejection of claim 6 incorporates and Larson further discloses:

> *- wherein the terminating event for the ring slot with a highest address allows the first slot in the ring to be processed first.* (col 3 lines 65 – 67 and col 4 lines 1 – 2, "The thread scheduler of the present invention requires that every thread have a period associated with the thread. The thread scheduler is rate monotonic; i.e., it assigns priorities based on the rate of the thread (shorter duration periods have higher priority).") priority of the thread is the ring slot with highest priority being the first slot.

Claims 12 - 15 are computer readable medium comprising instructions for executing the method of claims 4 - 7 above. They are therefore rejected under the same rational.

Conclusion

13.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure. .

TITLE: Method for time partitioned application scheduling in a computer operating system, US

6,754,690 B2

TITLE: Interrupt management system having batch mechanism for handling interrupt events, US

6,115,779

TITLE: Fault tolerant task dispatching, US 6,182,238

TITLE: Dynamically adjustable load-sharing circular queues, US 6,782,461 B2

TITLE: System for executing, scheduling, and selectively linking time dependent processes

based upon scheduling time thereof, US 4,989,133 B2

TITLE: Multi-computer system, US 4,123,794

TITLE: A firm real-time system implementation using commercial off-the-shelf hardware and

free software, Real-Time Technology and Applications Symposium, 1998. Proceedings. Fourth

IEEE 3-5 June 1998

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Abdullah-Al Kawsar whose telephone number is 571-270-3169.

The examiner can normally be reached on 7:30am to 5:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Chameli Das can be reached on 571-270-1392. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Abdullah Al Kawsar

CHAMELI DAS
SUPERVISORY PATENT EXAMINER

5/14/07